IN THE CLAIMS

1. **(Currently Amended)** A <u>policy-based dynamic</u> power management system for ~~dynamicaly managing power application to each of a plurality of devices in~~ a computer system, <u>the computer system including a plurality of devices, wherein</u> the power management system ~~comprising~~ <u>comprises</u>:

(a) a ~~flexible~~ clock generator circuit including at least one fixed rate clock signal oscillator, said generator circuit for generating ~~one or more~~ <u>a plurality of</u> clock ~~signals, wherein the frequency of each of said signals can be in a range from less than to greater than the frequency of said fixed rate clock signal; and~~ <u>signals;</u>

(b) a clock selector circuit ~~responsive to a rate of usage of each of said plurality of devices that directs a particular frequency of an output signal to be supplied~~ <u>for providing a selected one or more of the plurality of clock signals</u> to each of said plurality of ~~devices to maintain operation of each of said plurality of devices and minimize the total power being consumed by the computer system.~~ <u>devices; and</u>

<u>(c) a clock policy unit for monitoring operational state of the computer system and for selecting the one or more clock signals based on factors including a current state of operation of the computer system and one or more programmable policies, wherein the policies indicate desired clock frequencies associated with the current state of operation.</u>

2. **(Currently Amended)** The system of Claim 1 further comprising a static power management system for managing power application to each of said plurality of devices by withdrawing power from a device that is not currently active, and ~~re-applying power when said~~ <u>applying power to the device when the</u> device is needed to be active.

1   3.   **(Currently Amended)**   The system of Claim 2, wherein the static power

·2   management system includes a circuit for disconnecting ~~the address, and control data in and data~~

3   ~~out pins of a component of the computer system in order to reduce the power consumption of the~~

4   ~~computer system~~ <u>certain pins of one or more of the plurality of devices</u>.

1   4.   **(Currently Amended)**   The system of Claim 1, wherein the clock generator

2   circuit includes a first oscillator that generates a first clock signal, a second clock oscillator that

3   generates a second clock signal, and a programmable clock circuit that generates a third clock

4   signal based on the second clock signal, wherein said clock ~~select~~ <u>selector</u> circuit selects one of

5   the first, second and third clock signals ~~that is supplied to a portion of the computer system~~ to

6   provide ~~that~~ <u>a</u> portion of the computer system with a ~~predetermined~~ <u>desired</u> clock signal.

1   5.   **(Currently Amended)**   The system of Claim 4, wherein the clock ~~select~~ <u>selector</u>

2   circuit includes a ~~clock~~ state machine for ~~determining the clock state of the computer system at a~~

3   ~~predetermined time and a clock policy circuit for generating control signals to the clock select~~

4   ~~circuit in order to output the appropriate clock signal~~ <u>monitoring the current operational state and</u>

5   <u>selecting the one or more clock signals.</u>

1   6.   **(Currently Amended)**   The system of Claim 5, wherein the ~~clock state machine~~

2   ~~provides~~ <u>current operational state is selected from a group of states including</u> an idle state when

3   the computer system is waiting for an input, a busy state when the computer system is

4   performing a task, a sleep state when the computer system has timed out due to inactivity and a

5   dead state when power has failed to the computer system.

1   7.   **(Currently Amended)**   The system of Claim 6, wherein the clock ~~select~~

·2   <u>generator</u> circuit includes a circuit that generates ~~a system clock~~ <u>first and second system clocks</u>, a

3   ~~circuit that generates a processor clock and a circuit that generates a co-processor clock~~ wherein

4   each of the clocks is independently and simultaneously operable.

1   8.   **(Currently Amended)**   The system of Claim ~~6, wherein,~~ <u>7, wherein the</u>

2   <u>programmable clock circuit includes a phase locked loop, the computer system includes first and</u>

3   <u>second processors and,</u> during the idle state, the clock ~~select circuit generates no clock for~~

4   <u>selector circuit:</u>

5   <u>disconnects clocks from</u> the phase locked loop and ~~co-processor so that they are off, the~~

6   ~~clock select circuit generates the first clock signal for the processor so that the~~

7   ~~processor is clocked at a slow rate and the clock select circuit generates a high rate~~

8   ~~clock for an interrupt circuit so that the interrupt circuit is active and can increase the~~

9   ~~clock frequency for the computer system~~ <u>the second processor;</u>

10   <u>and connects the first processor to the fist system clock.</u>

1   9.   **(Currently Amended)** The system of Claim 6 <u>7</u>, wherein, during the busy state,

2   the clock ~~select~~ <u>selector</u> circuit ~~generates a high-rate clock signal for the processor, the co-~~

3   ~~processor and the interrupt circuits~~ <u>connects clocks to the phase locked loop and the second</u>

4   <u>processor and connects the first processor to the second system clock.</u>

1   10.   **(Currently Amended)** The system of Claim 6, wherein, during the sleep state,

2   the clock ~~select~~ <u>selector</u> circuit ~~generates no clock signal for the processor and the co-processor~~

3   <u>disconnects clocks from the first and second processors.</u>

1   11.   (Original) The system of Claim 5, wherein the clock state machine is controlled

2   by an interrupt signal and software commands.

1   12.   (Original) The system of Claim 4, wherein the programmable clock circuit

2   generates a fourth clock signal.

1   13.   (Original) The system of Claim 12, wherein the first, second, third and fourth

2   clock signals have different frequencies.

1   14.   **(Currently Amended)** The system of Claim 13, wherein the first clock signal

2   frequency is 32 kHz, the second clock signal frequency is 24 ~~MhZ~~ <u>MHz</u>, the third clock signal

3   frequency is 33 ~~MhZ~~ <u>MHz</u> and the fourth clock signal frequency is 66 ~~MhZ~~ <u>MHz</u>.

1   15.   (Previously presented) The system of Claim 4 further comprising a time of day

2   circuit that generates time of day clock signals based on the first clock signal.

1   16.   (Previously presented) The system of Claim 4, wherein the clock select circuit

2   includes means for dynamically changing the clock frequency applied to each device of the

3   computer system based on the task being performed by the computer system.

1   17.   (Previously presented) The system of Claim 4, wherein the clock select circuit

2   includes a multiplexer.

1   18.   (Previously presented) The system of Claim 4, wherein the programmable clock

2   generator further includes a prescalar unit and a post scalar unit whose outputs are fed into a

3   phase locked loop that generates a third clock signal and a fourth clock signal having different

4   frequencies.

1   19.   **(Currently Amended)** A <u>policy-based dynamic</u> power management method for

2   a computer system having a plurality of devices wherein ~~power is dynamically supplied to each~~

3   ~~device,~~ the power management method ~~comprising~~ <u>comprises</u>:

4   (a)   generating ~~by a clock generator having a crystal oscillator one or more~~

5   ~~different~~ <u>a plurality of</u> clock signals wherein each ~~clock signal~~ <u>of the plurality of clock</u>

6   <u>signals</u> has a different predetermined ~~frequency,~~ <u>frequency;</u> ~~and   wherein   said~~

7   ~~predetermined frequencies are selectable in a frequency range from less than to greater~~

8   ~~than a frequency of said crystal oscillator;~~ and

9

10   (b)   <u>supplying one or more of the plurality of clock signals to each of the</u>

11   <u>plurality of devices, wherein the one or more clock signals are selected based on control</u>

12   <u>signals received from a clock policy unit;</u>

13

14   <u>(c)</u> ~~(b)   dynamically~~ adjusting the <u>frequency of the one or more</u> clock <u>signals</u>

15   ~~supplied to each device of the computer system in order to reduce the total power being~~

16   ~~consumed by the computer system.~~ <u>responsive to changes in the control signals, wherein</u>

17   <u>the clock policy unit configures the control signals based on factors including a</u>

18   <u>current state of operation of the computer system and one or more</u>

19   <u>programmable policies, wherein the policies indicate desired clock</u>

20   <u>frequencies associated with the current state of operation.</u>

1   20.   **(Currently Amended)** The method of Claim 19 further comprising withdrawing

2   power from <u>certain</u> devices ~~that are not currently active~~ to reduce ~~the~~ power consumption of the

3   computer system ~~so as to provide static power management~~.

1   21.   **(Currently Amended)** The method of Claim 20, wherein said withdrawing

.2   power includes disconnecting ~~the an address, and~~ address, control <u>and</u> data in and data out pins

3   of ~~a device~~ <u>one or more of the plurality of devices</u> ~~of the computer system in order to reduce the~~

4   ~~power consumption of the computer system~~.

1   22.   **(Currently Amended)** The method of Claim 19, wherein said generating further

2   includes generating a first clock signal with a first oscillator, generating a second clock signal

3   using a second oscillator, generating a third clock signal based on the second clock signals, and

4   selecting by a programmable clock select circuit one of the first, second and third clock signals

5   ~~that is supplied to~~ <u>to supply</u> a portion of the computer system ~~to provide that portion of the~~

6   ~~computer system with a predetermined clock signal~~.

1   23.   **(Currently Amended)** The method of Claim 22, wherein said selecting further

2   includes determining by a state machine the clock state of the computer system at a

3   predetermined time and generating control signals to the clock select circuit in order to ~~output~~

4   ~~the appropriate~~ <u>select a corresponding</u> clock signal.

1   24.   (Previously presented) The method of Claim 23, wherein said selecting further

2   includes an idle state wherein the computer system is waiting for an input, a busy state wherein

3   the computer system is performing a task, a sleep state wherein the computer system has timed

4   out due to inactivity and a dead state wherein power has failed to the computer system.

1   25.   (Previously presented) The method of Claim 24, wherein said selecting further

2   includes generating a system clock, generating a processor clock and generating a co-processor

3   clock wherein each of the clocks is independently and simultaneously operable.

1   26.   (Previously presented) The method of Claim 24, wherein during the idle state, no

2   clock signal is provided to the phase locked loop and co-processor so that they are off, and

3   generating the first clock signal for the processor so that the processor is clocked at a slow rate

4   and generating a high rate clock for an interrupt circuit so that the interrupt circuit is active and

5   can increase the clock frequency for the computer system.

1   27.   (Previously presented) The method of Claim 24, wherein during the busy state, a

2   high rate clock signal is applied to the processor, the co-processor and the interrupt circuits.

1   28.   (Previously presented) The method of Claim 24, wherein during the sleep state,

2   no clock signal is applied to the processor and the co-processor.

1   29.   (Original) The method of Claim 23, wherein the clock state machine is controlled

2   by an interrupt signal and software commands.

1   30.   (Original) The method of Claim 22 further comprising generating a fourth clock

2   signal.

1   31.   (Original) The method of Claim 30, wherein the first, second, third and fourth

2   clock signals have different frequencies.

1   32.   **(Currently Amended)** The method of Claim 31, wherein the first clock signal

.2   frequency is 32 kHz, the second clock signal frequency is 24 ~~MhZ~~ MHz, the third clock signal

3   frequency is 33 ~~MhZ~~ MHz and the fourth clock signal frequency is 66 ~~MhZ~~ MHz.

1   33.   (Previously presented) The method of Claim 22 further comprising generating

2   time of day clock signals based on the first clock signal.

1   34.   (Previously presented) The method of Claim 22, wherein the clock select circuit

2   further includes means for dynamically changing the clock frequency applied to each device of

3   the computer system based on the task being performed by the computer system.

1   35.   (Previously presented) The method of Claim 22, wherein the clock select circuit

2   includes a multiplexer.

1   36.   (Previously presented) The method of Claim 22, wherein the programmable

2   clock circuit further includes a prescalar unit and a post scalar unit having outputs that are fed

3   into a phase locked loop that generates a third clock signal and a fourth clock signal having

4   different frequencies.

1   37.   **(Currently Amended)** A flexible clock generator, comprising:

2   a first oscillator that generates a first clock signal;

3   a second clock oscillator that generates a second clock signal;

4   a programmable clock circuit that generates a third clock signal based on the second

5   clock signal wherein a frequency of said third clock signal can be in a range from less than to

6   greater than a frequency of said second clock signal; and

7   a clock select circuit that selects one of the first, second and third clock signals that is

8   supplied to a portion of the computer system to provide that portion of the computer system with

9   a predetermined clock ~~signal.~~ signal, wherein the clock select circuit selects clock signals based

10   on factors including a current state of operation of the computer system and one or more

11   programmable policies, wherein the policies indicate desired clock frequencies associated with

12   the current state of operation.

1   38.   (Previously presented) The generator of Claim 37, wherein the clock select

2   circuit includes a clock state machine for determining the clock state of the computer system at a

3   predetermined time and a clock policy circuit for generating control signals to the clock select

4   circuit in order to output the appropriate clock signal.

1   39.   (Previously presented) The generator of Claim 38, wherein the clock state

2   machine provides an idle state wherein the computer system is waiting for an input, a busy state

3   wherein the computer system is performing a task, a sleep state wherein the computer system has

4   timed out due to inactivity and a dead state wherein power has failed to the computer system.

1   40.   (Previously presented) The generator of Claim 39, wherein the clock select

2   circuit further includes a circuit that generates a system clock, a circuit that generates a processor

3   clock and a circuit that generates a co-processor clock wherein each of the clocks is

4   independently and simultaneously operable.

1   41.   **(Currently Amended)** The generator of Claim 39, wherein, during the idle state,

2   the clock select circuit ~~generates no clock for the~~ disconnects clocks from the phase locked loop

3   and co-processor ~~so that they are off~~, the clock select circuit generates the first clock signal for

4   the processor so that the processor is clocked at a slow rate and the clock select circuit generates

5   a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the

6   clock frequency for the computer system.

1   42.   (Original) The generator of Claim 39, wherein, during the busy state, the clock

2   select circuit generates a high rate clock signal for the processor, the co-processor and the

3   interrupt circuits.

1   43.   (Original) The generator of Claim 39, wherein, during the sleep state, the clock

2   select circuit generates no clock signal for the processor and the co-processor.

1   44.   (Original) The generator of Claim 38, wherein the clock state machine is

2   controlled by an interrupt signal and software commands.

1   45.   (Original) The generator of Claim 37, wherein the programmable clock circuit

2   generates a fourth clock signal.

1   46.   (Original) The generator of Claim 45, wherein the first, second, third and fourth

2   clock signals have different frequencies.

1   47.   **(Currently Amended)** The generator of Claim 46, wherein a frequency of the

2   first clock signal is 32 kHz, a frequency of the second clock signal is 24 ~~MhZ~~ MHz, a frequency

3   of the third clock signal is 33 ~~MhZ~~ MHz and a frequency of the fourth clock signal is 66 ~~MhZ~~

4   MHz.

1   48.   (Previously presented) The generator of Claim 37 further comprising a time of

2   day circuit that generates time of day clock signals based on the first clock signal.

1   49.   (Previously presented) The generator of Claim 37, wherein the clock select

2   circuit includes means for dynamically changing the clock frequency applied to each component

3   of the computer system based on a task being performed by the computer system.

1   50.   (Previously presented) The generator of Claim 37, wherein the clock select

2   circuit includes a multiplexer.

1   51.   (Previously presented) The generator of Claim 37, wherein the programmable

2   clock generator includes a prescalar unit and a post scalar unit whose outputs are fed into a phase

3   locked loop that generates a third clock signal and a fourth clock signal having different

4   frequencies.

1   52.   **(Currently Amended)** A power management method for a computer system

2   comprising:

3   dynamically managing power application to each of a plurality of devices of said

4   computer system including

5   a)   first sensing a current operational usage of <u>said</u> each ~~said~~ device; ~~and~~

6   b)   adjusting a frequency of a clock signal from a clock generator to <u>said</u> each ~~said~~

7   device, said frequency in proportion to said usage, wherein said clock signal is supplied by a

8   flexible clock generator including at least one oscillator, and wherein said generator ~~can output~~

9   <u>provides</u> at least one signal having a frequency adjustable from less than to greater than a

10   frequency of said at least one ~~oscillator.~~ <u>oscillator; and</u>

11   <u>c)   responsive to interrupt and software command, modifying current operational</u>

12   <u>usage of one or more of said each device.</u>

1   53.   (**Currently Amended**) The method of Claim 52, further comprising:

2   statically managing power application to <u>said</u> each ~~said~~ device including

3   a)   second sensing to determine if a system device is being used;

4   b)   withdrawing power including a clock signal from a device, if said device

5   is not being used;

6   c)   determining if an unpowered device is needed; and

7   d)   applying power including a clock signal to said unpowered device if said

8   device is needed.

1   54.   (**Currently Amended**) The method of Claim 53 further comprising:

2   optimizing by a device controller to manage said dynamic power application to <u>said</u> each

3   device for a lowest computer system power consumption consistent with required operation of

4   <u>said</u> each ~~said~~ device.

1   55.   (Previously presented) The method of Claim 53 wherein said withdrawing power

2   includes gating off logic and a clock signal to a device, and applying power includes reapplying

3   logic and a clock signal to said device.